CLAIMS

1. An electronic circuit for updating a block of memory cells, the electronic circuit comprising:

a block of memory cells;

a controller for simultaneously erasing a current value stored in the block of memory cells;

a data latch for receiving a new value to be written to at least one cell in the block of memory cells;

a program load bank coupled to the controller and the data latch for programming the cell in the block of memory cells individually; and

control logic couple to the controller and the data latch, the control logic for selecting the cell in the block of memory cells for enabling the controller to erase the current value stored therein and for programming the new value therein;

whereby the control logic is governed by a result of a comparison between the new value to be written in the cell of the block of memory cells with the current value stored in the cell of the block of memory cells.

2. The electronic circuit according to claim 1, wherein the control logic further includes:

at least one combinatorial circuit, wherein the combinatorial circuit receives as inputs

the current value stored in the cell and

the new value to be written in the cell, and

the combinatorial circuit provides as outputs

an erase-enabling signal for governing the controller, and

a program-enabling signal for governing the program load bank.

3. The electronic circuit according to claim 2, further comprising:

a latch for storing the current value read from the cell of the block of memory cells and wherein the latch provides the current value as input to the combinatorial circuit.

4. The electronic circuit according to claim 1, wherein the block of memory cells consists of a non-volatile register for storing protection information for a matrix of memory cells.

5. The electronic circuit according to claim 2, wherein the block of memory cells consists of a non-volatile register for storing protection information for a matrix of memory cells.

6. The electronic circuit according to claim 3, wherein the block of memory cells consists of a non-volatile register for storing protection information for a matrix of memory cells.

7. The electronic circuit according to any claim 1, wherein the control logic includes:

an erase-enabling means responsive to the current value and to the new value for enabling the controller, when an erase operation is required, to reach the new value from the current value; and

a program-enabling means responsive to the new value and to an up-top-date current value stored in the memory cells after the possible erase operation for enabling the programming load bank, when a program operation is required, to reach the new value from the up-to-date current value.

8. The electronic circuit according to any claim 2, wherein the control logic includes:

an erase-enabling means responsive to the current value and to the new value for enabling the controller, when an erase operation is required, to reach the new value from the current value; and

a program-enabling means responsive to the new value and to an up-top-date current value stored in the memory cells after the possible erase operation for enabling the programming load bank, when a program operation is required, to reach the new value from the up-to-date current value.

9. The electronic circuit according to any claim 3, wherein the control logic includes:

an erase-enabling means responsive to the current value and to the new value for enabling the controller, when an erase operation is required, to reach the new value from the current value; and

a program-enabling means responsive to the new value and to an up-top-date current value stored in the memory cells after the possible erase operation for enabling the programming load bank, when a program operation is required, to reach the new value from the up-to-date current value.

10. The electronic circuit according to any claim 6, wherein the control logic includes:

an erase-enabling means responsive to the current value and to the new value for enabling the controller, when an erase operation is required, to reach the new value from the current value; and

a program-enabling means responsive to the new value and to an up-top-date current value stored in the memory cells after the possible erase operation for enabling the programming load bank, when a program operation is required, to reach the new value from the up-to-date current value.

11. The electronic circuit according to any claim 8, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell has the current value programmed therein and the new value is equivalent to a value after the cell is erased; and

wherein the program-enabling means includes logic gates for asserting the program-enabling signal when the cell with an up-to-date current value is required to be erased and the new value programmed therein.

12. The electronic circuit according to any claim 9, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell has the current value programmed therein and the new value is equivalent to a value after the cell is erased; and

wherein the program-enabling means includes logic gates for asserting the program-enabling signal when the cell with an up-to-date current value is required to be erased and the new value programmed therein.

13. The electronic circuit according to any claim 10, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell has the current value programmed therein and the new value is equivalent to a value after the cell is erased; and

wherein the program-enabling means includes logic gates for asserting the program-enabling signal when the cell with an up-to-date current value is required to be erased and the new value programmed therein.

14. The electronic circuit, according to claim 1, wherein the control logic includes erase-enabling means responsive to the current value and to the new value for enabling the erasing controls when an erase operation is required to reach the new value from the current value, and

wherein the program-enabling means is responsive to the erase-enabling means, to the new value and to the current value for enabling the programming means when a program operation is required to reach the new value from the current value or when the erasing means has been enabled and the cell is programmed with the new value.

15. The electronic circuit, according to claim 2, wherein the control logic includes erase-enabling means responsive to the current value and to the new value for enabling the erasing controls when an erase operation is required to reach the new value from the current value, and

wherein the program-enabling means is responsive to the erase-enabling means, to the new value and to the current value for enabling the programming means when a program operation is required to reach the new value from the current value or when the erasing means has been enabled and the cell is programmed with the new value.

16. The electronic circuit, according to claim 3, wherein the control logic includes erase-enabling means responsive to the current value and to the new value for enabling the erasing controls when an erase operation is required to reach the new value from the current value, and

wherein the program-enabling means is responsive to the erase-enabling means, to the new value and to the current value for enabling the programming means when a program operation is required to reach the new value from the current value or when the erasing means has been enabled and the cell is programmed with the new value.

17. The electronic circuit, according to claim 6, wherein the control logic includes erase-enabling means responsive to the current value and to the new value for enabling the erasing controls when an erase operation is required to reach the new value from the current value, and

wherein the program-enabling means is responsive to the erase-enabling means, to the new value and to the current value for enabling the programming means when a program operation is required to reach the new value from the current value or when the erasing means has been enabled and the cell is programmed with the new value.

18. The electronic circuit, according to claim 15, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell is programmed with the current value and the new value in the is erased, and wherein the program-enabling means includes one or more logic gates for asserting the program-enabling signal when the current value in the cell is erased and the cell is programmed with the new value or when the erase-enabling signal is asserted and the cell is programmed with the new value.

19. The electronic circuit, according to claim 16, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell is programmed with the current value and the new value in the is erased, and wherein the program-enabling means includes one or more logic gates for asserting the program-enabling signal when the current value in the cell is erased and the cell is programmed with the new value or when the erase-enabling signal is asserted and the cell is programmed with the new value.

20. The electronic circuit, according to claim 17, wherein the erase-enabling means includes logic gates for asserting the erase-enabling signal when the cell is programmed with the current value and the new value in the is erased, and wherein the program-enabling means includes one or more logic gates for asserting the program-enabling signal when the current value in the cell is erased and the cell is programmed with the new value or when the erase-enabling signal is asserted and the cell is programmed with the new value.

21. A flash memory device comprising:

a matrix of memory cells;

a block of non-volatile memory cells for storing protection information for the matrix of memory cells;

a controller for simultaneously erasing a current value stored in the block of non-volatile memory cells;

a data latch for receiving a new value to be written to at least one cell in the block of non-volatile memory cells;

a program load bank coupled to the controller and the data latch for programming the cell in the block of non-volatile memory cells individually; and

control logic couple to the controller and the data latch, the control logic for selecting at least one cell in the block of non-volatile memory cells for enabling the controller to erase the current value stored therein and for programming one or more of the non-volatile memory cells therein with the new value;

whereby the control logic is governed by a result of a comparison between the new value to be written in the cell of the block of non-volatile memory cells with the current value stored in the cell of the block of non-volatile memory cells.

22. A method of updating a block of memory cells, the method comprising:

storing a current value in a block of memory cells;

receiving a new value to be written in the memory cells; and

enabling an erasing the block of memory cells simultaneously and enabling a programming of the memory cells individually according to a comparison between a new value to be written and the current value.